Failure Modes, Effects and Diagnostic Analysis

Project:
Surge protective devices DEHNpipe

Customer:
DEHN + SÖHNE GmbH + Co. KG.
Neumarkt
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Management summary

This report summarizes the results of the hardware assessment carried out on the surge protective devices DEHNpipe in the versions listed in the drawings referenced in section 2.4.1. Table 1 gives an overview of the different configurations that belong to the considered surge protective devices DEHNpipe.

The hardware assessment consists of a Failure Modes, Effects and Diagnostics Analysis (FMEDA). A FMEDA is one of the steps taken to achieve functional safety assessment of a device per IEC 61508. From the FMEDA, failure rates are determined and consequently the Safe Failure Fraction (SFF) can be calculated for a subsystem. For full assessment purposes all requirements of IEC 61508 must be considered.

Table 1: Configuration overview DEHNpipe

DPI ME 24 N A2G	For unbalanced interfaces with thread npt ½" (outside/outside). Earth conductor led through. Max. continuous operating voltage U_C: 24.5 VAC / 34.8 VDC
DPI MD 24 M 2S	For 4-20 mA interfaces with thread M20 x 1.5 (inside/outside). Option of direct, indirect or no shield earthing. Max. continuous operating voltage U_C: 24.5 VAC / 34.8 VDC
DPI MD EX 24 M 2	Surge arrester for protecting intrinsically safe circuits and bus systems. Low-capacitance, energy-coordinated protective circuit with insulation resistance > 500 V to earth. Max. continuous operating voltage U_C: 24.5 VAC / 34.8 VDC
DPI CD EXI 24 M DPI CD EXI 24 N	Surge arrester for protecting intrinsically safe circuits and bus systems. Low-capacitance, energy-coordinated protective circuit with insulation resistance > 500 V to earth. Max. continuous operating voltage U_C: 22.6 VAC / 32 VDC
DPI CD EXD 24 M DPI CD EXD 24 N	Flameproof surge arrester for use in potentially explosive atmospheres for protecting measuring circuits and bus systems. Low-capacitance, energy-coordinated protective circuit with insulation resistance > 500 V to earth. Max. continuous operating voltage U_C: 22.6 VAC / 32 VDC
DPI CD EXD 230 24 M DPI CD EXD 230 24 N	Flameproof surge arrester for use in potentially explosive atmospheres for combined protection of measuring circuits and power supplies. Protection of data side (measuring circuit) Max. continuous operating voltage U_C: 22.6 VAC / 32 VDC Protection of power side (power supply) Max. continuous operating voltage U_C: 255 VAC
DPI CD EXI+D 2x24 M DPI CD EXI+D 2x24 N	Intrinsically safe and flameproof surge arrester for use in potentially explosive atmospheres for protection of two measuring circuits. Max. continuous operating voltage UC: 25.4 VAC / 36 VDC
DPI CD EXI+D 2x48 M DPI CD EXI+D 2x48 N	Intrinsically safe and flameproof surge arrester for use in potentially explosive atmospheres for protection of two measuring circuits. Max. continuous operating voltage UC: 41 VAC / 58 VDC
DPI CD HF EXD 5 M	Flameproof surge arrester for use in potentially explosive atmospheres for protection of a measuring circuit and bus system. Max. continuous operating voltage UC: 4.2 VAC / 6 VDC

For safety applications only the described configurations were considered. All other possible variants or electronics are not covered by this report.

Surge protective devices are not considered to be elements according to IEC 61508-4 section 3.4.5 as they are not performing one or more element safety functions. Therefore there is no need to calculate a SFF (Safe Failure Fraction). Only the interference on a safety functions needs to be considered. This interference is expressed in a contribution to the overall PFD_{AVG} / PFH.

The failure rates used in this analysis are from the *exida* Electrical & Mechanical Component Reliability Handbook for Profile 2.

The following tables show how the above stated requirements are fulfilled under worst-case assumptions.

Table 2: DPI ME 24 N A2G – Failure rates [1]

	***exida* Profile 2**	
	Analysis 1 [2]	**Analysis 2 [3]**
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**7**
Fail Dangerous Undetected (λ_{DU})	**9**	**2**
No effect	19	19
No part	0.5	0.5
Total failure rate (safety function)	**12 FIT**	**12 FIT**
MTBF	**3694 years**	**3694 years**

[1] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[2] Analysis 1 represents a worst-case analysis.

[3] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 3: DPI MD 24 M 2S – Failure rates [4]

	exida Profile 2	
	Analysis 1 [5]	**Analysis 2 [6]**
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**3**	**3**
Fail Dangerous Detected (λ_{DD})	**0**	**4**
Fail Dangerous Undetected (λ_{DU})	**6**	**2**
No effect	18	18
No part	21	21
Total failure rate (safety function)	**9 FIT**	**9 FIT**
MTBF	**2408 years**	**2408 years**

[4] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[5] Analysis 1 represents a worst-case analysis.

[6] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 4: DPI MD EX 24 M 2 – Failure rates [7]

	exida Profile 2	
	Analysis 1 [8]	**Analysis 2 [9]**
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**4**
Fail Dangerous Undetected (λ_{DU})	**6**	**2**
No effect	18	18
No part	21	21
Total failure rate (safety function)	**8 FIT**	**8 FIT**
MTBF	**2434 years**	**2434 years**

[7] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[8] Analysis 1 represents a worst-case analysis.

[9] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 5: DPI CD EXI(D) 24 M(N) – Failure rates [10]

	exida Profile 2	
	Analysis 1 [11]	**Analysis 2 [12]**
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**1**	**1**
Fail Dangerous Detected (λ_{DD})	**0**	**4**
Fail Dangerous Undetected (λ_{DU})	**21**	**17**
No effect	34	34
No part	20	20
Total failure rate (safety function)	**22 FIT**	**22 FIT**
MTBF	**1500 years**	**1500 years**

[10] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[11] Analysis 1 represents a worst-case analysis.

[12] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 6: DPI CD EXD 230 24 M(N) – Failure rates [13]

	exida Profile 2	
	Analysis 1 [14]	**Analysis 2 [15]**
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**80**	**80**
Fail Dangerous Detected (λ_{DD})	**0**	**4**
Fail Dangerous Undetected (λ_{DU})	**21**	**17**
No effect	38	38
No part	20	20
Total failure rate (safety function)	**101 FIT**	**101 FIT**
MTBF	**821 years**	**821 years**

[13] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[14] Analysis 1 represents a worst-case analysis.

[15] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 7: DPI CD EXI+D 2x24 M(N) – Failure rates [16]

	exida Profile 2	
	Analysis 1 [17]	**Analysis 2 [18]**
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**1**	**1**
Fail Dangerous Detected (λ_{DD})	**0**	**4**
Fail Dangerous Undetected (λ_{DU})	**5**	**1**
No effect	18	18
No part	21	21
Total failure rate (safety function)	**6 FIT**	**6 FIT**
MTBF	**2565 years**	**2565 years**

[16] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[17] Analysis 1 represents a worst-case analysis.

[18] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 8: DPI CD EXI+D 2x48 M(N) – Failure rates [19]

	exida Profile 2	
	Analysis 1 [20]	**Analysis 2 [21]**
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**1**	**1**
Fail Dangerous Detected (λ_{DD})	**0**	**1**
Fail Dangerous Undetected (λ_{DU})	**7**	**6**
No effect	19	19
No part	21	21
Total failure rate (safety function)	**8 FIT**	**8 FIT**
MTBF	**2403 years**	**2403 years**

[19] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[20] Analysis 1 represents a worst-case analysis.

[21] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.

Table 9: DPI CD HF EXD 5 M – Failure rates [22]

	exida Profile 2	
	Analysis 1 [23]	**Analysis 2 [24]**
Failure category	**Failure rates (in FIT)**	**Failure rates (in FIT)**
Fail Safe Detected (λ_{SD})	**0**	**0**
Fail Safe Undetected (λ_{SU})	**2**	**2**
Fail Dangerous Detected (λ_{DD})	**0**	**4**
Fail Dangerous Undetected (λ_{DU})	**22**	**18**
No effect	34	34
No part	1	1
Total failure rate (safety function)	**24 FIT**	**24 FIT**
MTBF	**1951 years**	**1951 years**

The failure rates are valid for the useful life of the surge protective devices DEHNpipe (see Appendix 2).

It is the responsibility of the Safety Instrumented Function designer to do calculations for the entire SIF. *exida* recommends the accurate Markov based exSILentia tool for this purpose.

Section 5 describes how to apply the results of the FMEDA.

[22] It is assumed that complete practical fault insertion tests can demonstrate the correctness of the failure effects assumed during the FMEDA.

[23] Analysis 1 represents a worst-case analysis.

[24] Analysis 2 represents an analysis with the assumption that line short circuits and short circuits to GND are detectable or do not have an effect.